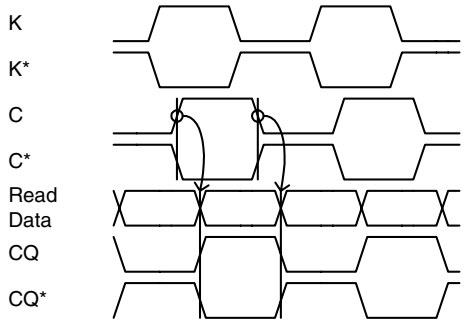

FIGURE 8.13 DDR SSRAM clocking.

proper phase with the memory controller's K/K*, thus saving it the complexity of dealing with a separate read clock domain. Such decisions are implementation specific and depend on the circuits and resources available.

Because of the high frequency of the DDR interface, bus turnaround time becomes an important design point. Idle time must be inserted onto a bidirectional data bus to enable the SRAM and memory controller time to disable their tri-state drivers when transitioning from reading to writing or vice versa. DDR SRAMs are manufactured in both *single* and *common I/O* (SIO and CIO) configurations to address turnaround timing. SIO DDR SRAMs feature two data buses—one dedicated for incoming write data and the other dedicated for outgoing read data. CIO devices feature a common bidirectional data bus. The latencies between address and data are identical between SIO and CIO devices. Write data begins on the first rising edge following the write command, and read data is returned beginning on the second falling edge following the read command. An LD* signal indicates an active read or write command. Figure 8.14 shows the timing for an SIO device in which bus turnaround is not an issue because of the dual unidirectional buses. Note that read data can overlap write data in the same clock cycle.

Commands can be issued continuously on an SIO device, because there is no possibility for data bus conflicts. A CIO device, however, requires at least one explicit idle cycle when transitioning from reading to writing, as shown in Fig. 8.15, because of the difference in data latencies for these two transactions. Without the idle cycle, write data would occur in the same cycle at the last two read words. CIO data sheets also warn that, at high frequencies, a second idle cycle may be necessary to prevent a bus conflict between the SRAM and the write data. The concern at high frequencies is that

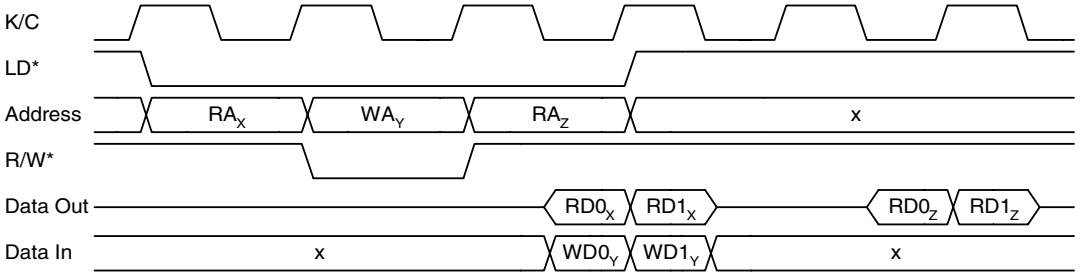

FIGURE 8.14 Separate I/O DDR SRAM read/write timing (burst length = 2).

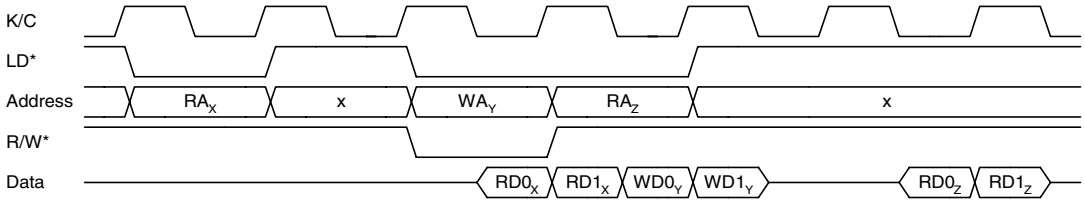

FIGURE 8.15 Common I/O DDR SRAM read/write timing (burst length = 2).

the SRAM may not be able to turn off its tri-state drivers in time for write data being driven immediately on the next cycle.

High data transfer rates are possible with CIO DDR SRAM in purely random transactions. Grouping multiple reads and writes into separate groups increases the available bandwidth by minimizing bus turnaround delays associated with read/write transitions. CIO devices have a distinct advantage in reduced signal count because of a single data bus. Balancing this out is the complexity of handling bus turnaround and somewhat reduced bandwidth in truly random transfer patterns.

SIO DDR SRAM provides a definite performance advantage in certain applications at the cost of additional signal and pin count. The concept of dual data interfaces was taken a step farther with the development of *quad data rate* ™ (QDR) SRAM technology, where the goal is to enable full utilization of the read and write data interfaces.* QDR devices are manufactured with fixed two- or four-word bursts. The address/control interface is designed so that enough commands can be issued to keep both data interfaces fully utilized. A four-word burst QDR SRAM is very similar to an SIO DDR SRAM if one were to be made with a four-word burst size. The difference is that, rather than having a R/W* select signal and an activation signal (LD*), the QDR devices implement separate read and write enables. A new command is presented during each clock cycle such that it takes two cycles to issue both a read and a write command. This frequency of commands matches perfectly with the four-word burst nature of the dual data interfaces. Each read or write command transfers four words at DDR, thereby occupying two whole clock cycles. Therefore, a read command can be issued once every two cycles, and it takes two cycles to execute. The same holds true for a write command. A two-word burst QDR SRAM differs from the four-word variety in that its address/control interface is dual rate to allow commands to be issued twice as fast to keep up with the shorter transfer duration of one cycle (two words at DDR complete in one whole cycle). Figure 8.16 shows the timing for a four-word burst QDR SRAM. If an application can make efficient use of a four-word

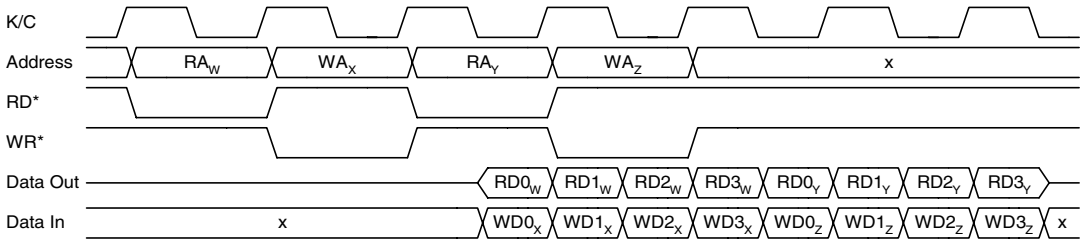

FIGURE 8.16 QDR SRAM read/write timing (burst length = 4).

* QDR is a trademark of Cypress, IDT, Micron Technology, NEC, and Samsung.